REMARKS

The Office Action mailed on October 3, 2001, has been received and reviewed. Claims 1 through 40 are currently pending in the application. Claims 1 through 23 and 36 through 40 stand rejected. Claims 24 through 35 have been withdrawn from consideration. Claims 24 through 35 have been canceled without prejudice or disclaimer. Claims 1, 18 through 20, 22, 36 through 38, and 40 have been amended. New claims 41-49 have been added.

Reconsideration of the above-referenced application is respectfully requested.

Preliminary Amendment

Please note that a Preliminary Amendment was filed in the above-referenced application on April 9, 2001, but that the filing of the Preliminary Amendment was not acknowledged by the Office in either the outstanding Office Action or in the Office Action mailed on July 31, 2001. Should the Preliminary Amendment have failed for some reason to have been entered in the Office file, the undersigned attorney will be happy to have a true copy thereof hand-delivered to the Examiner.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 20, 22, and 36 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 20, 22, and 36 were amended in the Preliminary Amendment sent on April 9, 2001. In that process, preambles and other relevant information were inadvertently deleted from these claims. These typographical and editorial problems have been corrected in presently amended claims 20, 22, and 36, placing each of these claims in allowable form. Therefore, withdrawal of the rejection under the second paragraph of 35 U.S.C. § 112 is respectfully requested.

35 U.S.C. § 102(b) Anticipation Rejection

(A) Anticipation Rejection Based on Japanese Patent No. 10189653 to Kuniaki

Claims 1 through 5, 8, 10, 13 through 16, 36, and 40 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kuniaki (Japanese Patent No. 10189653).

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Also, "the identical invention must be shown in as complete detail as is contained in the claim." *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Kuniaki discloses a semiconductor element that can be easily subjected to flip-chip mounting to a circuit board and is suitable for high-density mounting. A plurality of electrodes 7, which are to be directly bonded to the circuit board by way of solder balls 11 placed on top thereof, are arranged centrally in-line on the surface 4a of the semiconductor element 3 (see, for example, the figure of Kuniaki). At least one support projection element 12, which will come into contact with the circuit board upon positioning the semiconductor element 3 thereover, is positioned on the element surface 4a in such a way as to prevent movement of the semiconductor element 3 along an axis extending through each of the solder balls on the center part of the element surface 4a. These support projection elements 12, arranged, for example, at the corners of the element surface 4a, are made in two pieces and have the same combined shape of the electrodes 7 and solder balls 11 mounted thereon. More specifically, these support projection elements 12 are made of auxiliary electrodes, having the same form and size as those of electrodes 7, and ball-shaped solder bumps 11, which also have the same form and size as the solder balls 11, mounted thereon. (Kuniaki, lines 12-29).

It is respectfully submitted that the Kuniaki reference does not contain the details that are contained in the presently amended independent claims 1 and 36. As to claim 1, the claimed invention comprises a method of forming at least one unitary stabilizer structure of any desired shape on the active surface of a flip-chip semiconductor so as to at least partially stabilize the die when disposed face down over a higher level substrate. As to claim 16, the claimed invention comprises a method for electrically bonding a flip-chip semiconductor device component having

a surface and conductive structures protruding therefrom to a substrate having contacts positioned correspondingly to said conductive structures that includes, among other things, forming at least one unitary stabilizer structure of any desired shape mounted to the semiconductor surface and disposed between this surface and substrate.

Therefore, since each and every element in independent claims 1 and 36 is not found or described in the cited reference in the identical detail as the presently claimed invention, they are not anticipated. Further, dependent claims 2-5, 8, 10, 13-16, and 40 are also not anticipated because the independent claims from which they depend are not anticipated.

Therefore, it is respectfully requested that the anticipation rejection of claims 1-5, 8, 10, 13-16, 36, and 40 under 35 U.S.C. § 102(b) be withdrawn.

(B) Anticipation Rejection Based on U.S. Patent No. 5,484,314 to Farnworth

Claim 19 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Farnworth (U.S. Patent No. 5,484,314). Applicant respectfully traverses this rejection, as hereinafter set forth.

Farnworth discloses a method for fabricating high aspect ratio support structures to function as spacers or subparts 18 in evacuated, flat-panel displays and the like, using a stereographic printing apparatus 30 readily available in the art. An electrode plate 21 is placed in a vat 34 with resin 18' on the top portion of a pedestal 32 with an adjustable height. (Farnworth, col. 3, line 49-64). The light-sensitive resin 18' forms a very thin layer superjacent the electrode plate 21. The depth of the layer is determined by the strength of the laser 31, and represents the height of the column support structure or spacer 18. A laser 31 is programmed to direct light or other radiant energy 33 toward the display electrode 21 in a pattern, representing the location of the micro-pillar spacer supports 18. The pattern is very accurately achieved due to the accuracy of the laser 31 and repeatable time after time. The resin material 18' hardens or cures wherever the light energy 33 impinges upon it. After the micro-pillar structures 18 have been completed, the electrode plate 21 and an anode plate 16 are attached and sealed, and a vacuum is created in the space between them, with the spacer structures 18 preventing implosion of the electrode plates upon each other. (Farnworth, col. 4, lines 15-51).

It is respectfully submitted that the Farnworth reference does not contain the details that are contained in the presently amended independent claim 19, i.e., a method of fabricating a semiconductor device component, comprising the steps of (1) placing a substrate of a semiconductor device having an active surface with contact pads exposed thereon in a horizontal plane; (2) recognizing a location and orientation of the substrate; and (3) stereolithographically forming on the active surface, between the contact pads and a peripheral edge of the substrate, at least one stabilizer of any desired shape having at least one layer of an electrically nonconductive semisolid material. Rather, Farnworth discloses a method for forming spacers, or support structures, in an area array over an array of emitter tips (electrode plate 21). Thus, these spacers would not be formed between contact pads and a peripheral edge of a substrate. Accordingly, it is respectfully submitted that Farnworth neither expressly nor inherently describes each and every element of amended independent claim 19. Therefore, withdrawal of the anticipation rejection of independent claim 19 under 35 U.S.C. § 102(b) is respectfully requested.

35 U.S.C. § 103(a) Obviousness Rejections

(A) Applicable Authority

The basic requirements of a *prima facie* case of obviousness are summarized in MPEP §2143 through §2143.03, *i.e.*, in order "to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success in combining the references. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the expectation of success must both be found in the prior art, and not based on Applicants' disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Further, in establishing a *prima facie* case of obviousness the initial burden is placed on the examiner. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found

the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). See also MPEP § 706.02(j) and § 2142.

The Supreme Court has established the standard of patentability to be applied in obviousness rejections in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). This standard has been summarized in MPEP § 2141 into four factual inquires including "(A) determining of the scope and contents of the prior art; (B) ascertaining the differences between the prior art and the claims in issue; (C) resolving the level of ordinary skill in the pertinent art; and (D) evaluating evidence of secondary considerations." It should be noted that, when applying the required patentability standards of *Graham,* the basic considerations which apply to obviousness rejections based on 35 U.S.C. § 103 should include the following principles of patent law: "(A) the claimed invention must be considered as a whole; (B) the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) reasonable expectation of success is the standard with which obviousness is determined." *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

(B) Obviousness Rejection Based on Japanese Patent No. 10189653 to Kuniaki in view of U.S. Patent No. 5,484,314 to Farnworth

Claims 6, 7, 11, 18, and 37 through 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuniaki (Japanese Patent No. 10189653) in view of Farnworth (U.S. Patent No. 5,484,314).

Each of claims 6, 7, and 11 is allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claims 37 through 39 are each allowable, among other reasons, as depending either directly or indirectly from claim 36, which is allowable.

Furthermore, it is respectfully submitted that a *prima facie* case of obviousness of dependent claims 6, 7, 11, 37, and 39 and independent claim 18 has not been made because there is no suggestion or motivation, either in the Kuniaki or Farnworth references or in the knowledge

generally available to one of ordinary skill in the art, to modify the references or to combine their teachings. *Vaeck*, supra. It is respectfully submitted that differences in the methods described in the Kuniaki and the Farnworth references have not been considered in determining the appropriateness of combining the two references to find obviousness in the present invention. Case law is clear that, while Patent Office classification of references may be some evidence of analogy, "the similarities and differences in structure and function of the inventions [should] carry far greater weight [in combining references for an obvious rejection]." *In re Ellis*, 476 F.2d 1370, 1372, 177 USPQ 526, 527 (CCPA 1973).

Kuniaki discloses a semiconductor element that that can be easily subjected to flip-chip mounting to a circuit board and is suitable for high-density mounting, using one or several support projections made of the same materials and shape as the electrodes and solder balls used to create the desired electrical contact between the chip and substrate, as well as a method for fabricating the semiconductor element.

Farnworth discloses a method for fabricating high aspect ratio support structures to function as spacers in evacuated, flat-panel displays and the like, using a stereographic printing apparatus. Farnworth is concerned with a variety of evacuated displays to be used in computers and the like, e.g., emitter displays, flat panel displays, such as liquid crystal displays, plasma displays, electro-luminescent displays, vacuum fluorescent displays, flat CRT displays, and other displays employing a pressure differential from outside of the display with respect to the inside of the display which requires support to prevent implosion (Farnworth, col. 4, lines 61-67).

In order to fabricate supports in accordance with the method described in Kuniaki, bond pads must first be provided on a semiconductor element so that a subsequently formed solder support can be secured to the semiconductor element. Solder reflow processes and, presumably, a solder mask and solder bath may be used to form the supports. Accordingly, the supports of Kuniaki could be formed at the same time as one another, as well as at the same time as the electrically conductive solder balls of a semiconductor element from which the spacers protrude. In contrast, the method of Farnworth employs an electrically nonconductive material and a stereographic process to fabrication spacers directly on a substrate. As the stereographic process requires that each of the spacers be separately fabricated, the spacers of Farnworth could not be fabricated simultaneously with one another or with any conductive structures that would protrude

from the substrate.

Moreover, the functions of the spacers or supports fabricated by the methods described in Kuniaki and Farnworth are completely different. Although a spacer-like device is made by Farnworth to prevent collapsing of two surfaces containing a vacuum there between and a spacer-like device is made in Kuniaki to stabilize electronic chips facing each other, that is the extent of the similarity in structure and function between the spacers formed by the two methods. Other than that, the Farnworth reference is not in the field of both the Kuniaki reference and the instant invention, it does not reasonably pertain to the problem being solved thereby, and it would not commend itself to an inventor's attention working in the art therein.

The Office is kindly reminded that "in order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). See also *In re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986); *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992) ("A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem."). Combining Kuniaki and Farnworth to find obviousness in the instant invention, neglecting the requirements of *Ellis*, *Oetiker*, and *Deminski*, supra, can only be justified by use of the benefit of impermissible hindsight vision afforded by the Applicant's claimed invention—a procedure contrary to current principles of patent law (cf. *Hodosh*, supra).

Further, as related to dependent claims 37 through 39, it should be noted that there are no protruding conductive structures disclosed in Farnworth so as to require the heights of the support structures to be shorter or taller than the minimum distance of these protruding structures as suggested in the Office Action (page 4, lines 11-12). Further, as discussed hereinabove with respect to the anticipation rejections, Kuniaki does not teach or disclose varying the height of the multi-component support projections because in Kuniaki those projections have the same height as the combined height of the electrodes and solder balls used to make them. Further, the supports of Kuniaki would not be useful for lengthening at least one conductive structure

because, in order to lengthen a conductive structure, the semiconductor element would have to be heated to a temperature that would at least partially reflow the material of the conductive structures, which temperature would also cause the supports to reflow, diminishing any structural integrity and shape of such structures that would cause the conductive structures to be lengthened as heat is applied thereto.

Therefore, a finding of obviousness of claims 37-39, i.e., (1) unitary stabilizer structures having a height less than the minimum distance the conductive structures protrude from the substrate surface (claim 37); (2) unitary stabilizer structure formed as to space the semiconductor surface from the substrate a distance greater than the minimum distance the conductive structures protrude from the substrate surface (claim 38); and (3) lengthening at least one of the unitary stabilizer structure (claim 39), is not based on a combination or suggestion to modify the prior art, but on the claimed invention.

Finally, the finding of obviousness of claims 6, 7, 11, 18, and 37 through 39 based on Official Notice that lengthening a conductive structure during bonding may be conventionally practiced in the semiconductor industry (Office Action, page 5, lines 1-7) is respectfully objected to. This objection is grounded on the fact that such an action is contrary to the required patentability standards of *Graham*, supra, and principles of patent law requiring that, when a determination of obviousness is made, "the claimed invention must be considered as a whole." *Hodosh, supra*. The Office is respectfully reminded that in establishing the differences between the prior art and a claimed invention "the question under 35 U.S.C. § 103 is not whether [a particular manufacturing method or process conventionally practiced in a industry] would have been obvious, but whether the claimed invention as a whole would have been obvious." *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983). In particular, when the subject matter recited in claim 39 is considered as a whole, it is apparent that the material from which the at least one unitary stabilizer is formed would have to, at the very least, maintain its length under conditions that would be necessary to length at least one conductive structure. In the case of a semiconductor element fabricated in accordance with the method of Kuniaki, this would mean that the support structures of Kuniaki would have to be formed from a material that would substantially retain its shape as the solder of the conductive structures is reflowed. Since the

conductive structures and supports of the semiconductor element formed in accordance with the method of Kuniaki comprise solder of the same type, it would not be possible to employ the supports to lengthen at least one of the conductive structures during bonding thereof.

Therefore, withdrawal of the obviousness rejection of claims 6, 7, 11, 18, and 37 through 39 under 35 U.S.C. § 103 is respectfully requested.

(C) Obviousness Rejection Based on Japanese Patent No. 10189653 to Kuniaki in view of U.S. Patent No. 5,636,696 to Liang et al.

Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuniaki (Japanese Patent No. 10189653) in view of Liang et al. (U.S. Patent No. 5,639,696).

Claim 17 is allowable, among other reasons, as depending from claim 1, which is allowable.

Further, it is respectfully submitted that a *prima facie* case of the obviousness of claim 17 has not been established.

Liang generally relates to the art of microelectronic integrated circuits, and more specifically to a microelectronic integrated circuit mounted on a circuit board with a solder column grid array interconnection, and a method of fabricating the column grid array. (Liang, col. 1, lines 10-14). An integrated circuit 60 is fabricated having a ball grid array formed thereon, including a ceramic laminate or other substrate 62 with a cavity 64. An integrated circuit chip 66 is mounted on one of the layers in the cavity 64, and interconnected with the substrate 62 by wire bonds 68 or the like and environmentally sealed by an encapsulant 70. An array of contact pads 72 is formed on the surface of the substrate 62, and an array of electrically conductive solder balls 74 is formed on the pads 72. The balls 74 are adhered to the pads 72 by applying flux to the pads 72, inserting the balls 74 into holes in a graphite fixture or boat in a conventional manner, aligning the pads 72 on top of the balls 74, and applying heat for a short period of time, causing the balls 74 to reflow onto the pads 72, and thereby become ohmically attached to the pads 72. The circuit 60 is then inverted and placed on top of a board 76 such that the solder balls 74 engage with conjugate terminals or contact pads 78 on the board 76 by applying heat again. The assembly is then inverted again such that the integrated circuit 60

extends downwardly from the circuit board 76. The circuit board 76 is held stationary, the solder balls 74 are again heated to reflow temperature, and the circuit 60 is urged by gravity to move downwardly relative to the board 76. This causes the solder balls 74 to be stretched into an elongated shape to form solder columns 80. The heat is then removed, and the solder solidifies into the column shapes. (*Id.*, col. 3, line 59 – col. 4, line 43).

In another embodiment of the same invention, a fixture 90 is disclosed to provide precise spacing between the integrated circuit 60 and the circuit board 76, and thereby a precise height for the solder columns 80. The height of the fixture 90 is selected such that its walls retain the circuit board 76 and the integrated circuit 60 abuts against the bottom when it has moved downwardly away from the circuit board 76 during solder reflow. This automatically provides a precise height for the solder columns 80. (*Id.*, col. 4, line 60 – col. 5, line 4). In yet another embodiment of the same invention, for situations when the integrated circuit 60 is so light that its weight is insufficient to cause it to move downwardly away from the circuit board 76 during solder reflow, a weight 92 is temporarily attached to the integrated circuit 60 by clips 94 or the like. The size of the weight 92 is selected to cause the integrated circuit 60 to move to a desired extent during reflow until it reaches a stopper 96 below the weight 92 such that the weight 92 will abut against the stopper 96 when the integrated circuit 60 has moved downwardly by the desired amount. (*Id.*, col. 5, lines 5-17).

It is respectfully submitted that the combination of Kuniaki and Liang cannot support a finding of obviousness for the present invention because the limitations of presently amended independent claim 1 are not taught by Kuniaki or Liang individually or in any combination thereof (*Vaeck*, supra), i.e., a method of forming at least one unitary stabilizer structure of any desired shape in the active surface of a flip-chip semiconductor, between the contact pads and a peripheral edge thereof, so as to at least partially stabilize the die when disposed face down over a higher level substrate. Thus independent claim 1 is not made obvious by the combination of Kuniaki and Liang and because "independent claim [1] is nonobvious under 35 U.S.C. 103, claim[17,] depending there from[, is also] nonobvious." *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Further, the combination of Liang (a method of flip-chip mounting microelectronic integrated circuits on a circuit board using cylindrical solder columns) and Kuniaki (a method of

stabilizing semiconductors substrates mounted by a flip-chip procedure by use of electrodes and spherical solder balls as support projections) only teaches a method of flip-chip mounting integrated circuits stabilized by use of electrodes and cylindrical solder columns as support projections. Considering the subject matter recited in claim 17 in its entirety, the combination of Liang and Kuniaki does not teach all of the limitations of claim 17 and therefore cannot support a finding of obviousness thereof. Dependent claim 17, in combination with dependent claim 15, adds to claim 1 the limitations of disposing at least one conductive structure on one bond pad of a flip-chip semiconductor die (claim 15) by applying one of a conductive pillar, a conductor filled epoxy pillar, and a structure of z-axis elastomer to the bond pad (claim 17). When viewed in combination with the limitations of claim 1, the invention claimed in claim 17 is a method of forming at least one unitary stabilizer structure of any desired shape in the active surface of a flip-chip semiconductor so as to at least partially stabilize the die when disposed face down over a higher level substrate wherein at least one conductive structure on one bond pad of a flip-chip semiconductor die is created by applying a conductive pillar, a conductor filled epoxy pillar, and a structure of z-axis elastomer to the bond pad. These limitations, considered as a whole, are not taught by Kuniaki or Liang individually or in any combination thereof (*cf. Stratoflex, and Gore, supra*).

Therefore, withdrawal of the obviousness rejection of claim 17 under 35 U.S.C. § 103 is respectfully requested.

(D) Obviousness Rejection Based on U.S. Patent No. 5,484,314 to Farnworth in view of U.S. Patent No. 5,870,220 to Migdal et al.

Claims 20 through 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Farnworth (U.S. Patent No. 5,484,314) in view of Migdal et al. (U.S. Patent No. 5,870,220).

Claims 20 through 23 are each allowable, among other reasons, as depending from claim 19, which is allowable.

In addition, it is respectfully submitted that a *prima facie* case as to the obviousness of claims 20 through 23 has not been established.

Migdal relates generally to three-dimensional (3D) scanning and measuring systems, and relates particularly to a portable 3D scanning system and method which facilitate acquisition and

storage of data relating to 3D profiles of objects for subsequent computer-aided data processing and reproduction of the 3D profiles of the objects by shape digitizing and adaptive mesh generation. (Migdal, col. 1, lines 6-12). Migdal discloses a system for rapidly scanning an object with a geometric light shape (such as a laser stripe), recording the shape of the reflected points of light by means of an image collector (such as a camera), and, by a triangulation technique that does not depend on the fixed direction of the light source relative to the camera, reconstructing the 3D shape of the object through a computer using the data points collected from the reflection of the laser stripes. With the collected data points, a user can, *inter alia*, create, display and manipulate an image of the 3D object on a computer, physically reproduce the object (through computer controlled milling machines and stereolithography), compress the data for easy transmission (such as over the Internet), or use the data in graphic manipulation systems (such as in 3D video animators). (*Id.*, col. 4, lines 3-22). It should be noted, unitary to the characterization found in the Office Action (page 6, line 1-3), Migdal does not disclose a stereolithography system. Reference to stereolithography was only made once in the entire patent (Id., col. 4, line 15) to illustrate an application of the scanning system taught and disclosed.

Moreover, Migdal includes no description of the use of a machine vision system to recognize the location on a substrate at which at least one stabilizer or, for that matter, any other structure is to be formed.

It is respectfully submitted that the combination of Migdal and Farnworth cannot support a finding of obviousness for the present invention because the limitations of presently amended independent claim 19 are not taught by Migdal or Farnworth individually or in any combination thereof (*Vaeck*, supra), i.e., a method of fabricating a semiconductor device component, comprising the steps of (1) placing a substrate of a semiconductor device having an active surface with contact pads exposed thereon in a horizontal plane; (2) recognizing a location and orientation of the substrate; and (3) stereolithographically forming on the active surface, between the contact pads and a peripheral edge of the substrate, at least one stabilizer of any desired shape having at least one layer of an electrically nonconductive semisolid material. Thus independent claim 19 is not made obvious by the combination of Migdal and Farnworth and because "independent claim [19] is nonobvious under 35 U.S.C. 103, claims [20-23] depending there

from[, are also] nonobvious." (*Fine*, supra).

It is respectfully submitted that differences between the method of the instant invention and those of combination of Migdal and Farnworth have not been considered in determining the appropriateness of combining the two references to find obviousness in the present invention. (*Ellis*, *Oetiker*, and *Deminski*, supra). Farnworth discloses a method for fabricating high aspect ratio support structures to function as spacers in evacuated, monitor displays, including emitter displays, flat panel displays, such as liquid crystal displays, plasma displays, electro-luminescent displays, vacuum fluorescent displays, flat CRT displays, and other displays employing a pressure differential from outside of the display with respect to the inside of the display which requires support to prevent implosion, using a stereographic printing apparatus. Migdal teaches a system for rapidly scanning an object with a geometric light shape, recording the shape of the reflected points of light by means of an image collector, and reconstructing the 3D shape of the object through a computer using the data points collected from the reflection of the laser stripes. Thus, the combination of Migdal and Farnworth would teach the use of a rapidly scanning system to aid in a stereographic printing apparatus to generate spacers to be used in a variety of evacuated displays in order to prevent implosion of adjacent surfaces due to the vacuum applied there between. There is no reasonable expectation that such a combination would be useful for recognizing a location on a substrate at which at least one stabilizer is to be formed.

Further, the combination of Migdal and Farnworth does not teach or suggest placing a substrate of a semiconductor device having an active surface with contact pads exposed thereon in a horizontal plane, recognizing a location and orientation of the substrate, and stereolithographically forming on the active surface, between the contact pads and a peripheral edge of the substrate, at least one stabilizer of any desired shape having at least one layer of an electrically nonconductive semisolid material (claim 19) by (1) storing data of at least one physical parameter of the substrate in computer memory, and using the stored data in conjunction with a machine vision system to recognize the location and orientation of the substrate and to form at least one stabilizer thereon (claim 20); (2) including in the computer memory at least one parameter of another semiconductor device component to which the substrate is to be attached (claim 21); (3) using the stored data, in conjunction with the machine vision system, to selectively form one layer of semisolid material stereolithographically on at

least one portion of the active surface of the substrate (claim 22); and (4) securing the substrate to a carrier prior to placing the substrate in a horizontal plane (claim 23). Therefore, combining Migdal and Farnworth to find obviousness in the instant invention can only be justified by use of the benefit of impermissible hindsight vision afforded by the subject matter disclosed and claimed in the above-referenced application.

Therefore, withdrawal of the obviousness rejection of claims 20-23 under 35 U.S.C. § 103 is respectfully requested.

(E) Obviousness Rejection Based on Japanese Patent No. 10189653 to Kuniaki

Claims 9 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuniaki (Japanese Patent No. 10189653).

Claims 9 and 12 are both allowable, among other reasons, as depending from claim 1, which is allowable.

Therefore, withdrawal of the obviousness rejection of claims 9 and 12 under 35 U.S.C. § 103 is respectfully requested.

ENTRY OF NEW CLAIMS

New claims 41 through 49 above should be entered because they are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1 through 23 and 36 through 49 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should it be determined that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact the undersigned attorney.

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Enclosure: Version of Specification with Markings to Show Changes Made
Version of Claims with Markings to Show Changes Made

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VERSION OF SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE

ABSTRACT OF THE DISCLOSURE

[Stabilizers to be disposed on a surface of a semiconductor device component and methods of fabricating and disposing the stabilizers on semiconductor device components. Semiconductor device components including the stabilizers are also disclosed, as well as assemblies wherein the stabilizers are disposed between a semiconductor device component and a higher level substrate.]One or more [of the] stabilizers are disposed on the surface of a semiconductor device component prior to bonding the same to a higher level substrate. Upon assembly of the semiconductor device component face down upon a higher level substrate and joining conductive structures[, such as solder structures,] between the contact pads of the semiconductor device component and corresponding contact pads of the higher level substrate, the stabilizers at least partially stabilize the semiconductor device component on the higher level substrate to [prevent tilting or tipping of the semiconductor device component relative to the higher level substrate] maintain a substantially parallel relation therebetween. The stabilizers can also be positioned and configured to define a minimum, substantially uniform distance between the semiconductor device component and the higher level substrate. The stabilizers may be preformed structures or [which are attached to a surface of a semiconductor device component. Alternatively, the stabilizers can be] fabricated on the surface of the semiconductor device component, such as by way of a [. A] stereolithographic method[of fabricating the stabilizers is disclosed. The stereolithographic method may include use of a machine vision system including at least one camera operably associated with a computer controlling a stereolithographic application of material so that the system may recognize the position and orientation of a substrate to which the material is to be applied].

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Twice amended) A method of forming a flip-chip semiconductor die, comprising:

providing at least one flip-chip semiconductor die having an active surface; and

forming at least one stabilizer securable to said active surface so as to protrude from said active surface, said at least one stabilizer being an unitary structure of any desired shape and configured to at least partially stabilize an orientation of said at least one flip-chip semiconductor die when disposed face down over a higher level substrate.

18. (Twice amended) A method of fabricating a semiconductor device component, comprising:

providing at least one semiconductor substrate with contact pads on an active surface thereof; and

sequentially forming on said active surface at least one stabilizer of any desired shape having a plurality of superimposed, contiguous, mutually adhered layers of photopolymer, said at least one stabilizer being configured to at least partially stabilize an orientation of the semiconductor device component upon being disposed face down over a higher level substrate.

19. (Twice amended) A method of fabricating a semiconductor device component, comprising:

placing at least one semiconductor substrate having an active surface with contact pads exposed thereon in a horizontal plane;

recognizing a location and orientation of said at least one substrate;

stereolithographically forming on said active surface, between one of said contact pads and a peripheral edge of said at least one substrate, at least one stabilizer of any desired shape comprising at least one layer of an electrically nonconductive semisolid material.

20. (Twice amended) The method of claim 19, further comprising storing data including at least one physical parameter of said at least one substrate in computer memory, and using the stored data in conjunction with a machine vision system to recognize said location and orientation of said at least one substrate and to form said at least one stabilizer thereon.

22. (Twice amended) The method of claim 20, further comprising using stored data, in conjunction with said machine vision system, to selectively form said at least one layer of semisolid material stereolithographically on at least one portion of said active surface of said at least one substrate.

36. (Twice amended) A method for electrically bonding a flip-chip semiconductor device component having a surface and conductive structures protruding from said surface to a substrate having contacts positioned correspondingly to said conductive structures, said method comprising:

forming at least one unitary stabilizer structure of any desired shape configured to be disposed between said surface and said substrate;

inverting and positioning said semiconductor device component on said substrate to contact said conductive structures to corresponding contacts; and

bonding said conductive structures to the corresponding contacts.

37. (Twice amended) The method of claim 36, wherein said forming at least one unitary stabilizer structure comprises forming said at least one unitary stabilizer structure to have a height less than a minimum distance said conductive structures protrude from said surface.

38. (Twice amended) The method of claim 36, wherein said forming at least one unitary stabilizer structure comprises forming said at least one unitary stabilizer structure to space said surface from said substrate a distance greater than a minimum distance at least one of said conductive structures protrudes from said surface.

39. (Twice amended) The method of claim 38, wherein said bonding comprises employing said at least one unitary stabilizer to lengthen [lengthening] at least one of said conductive structures.

40. (Twice amended) The method of claim 36, wherein said forming at least one unitary stabilizer structure comprises configuring said at least one unitary stabilizer structure to be positioned between a periphery of said surface of said semiconductor device component and said conductive structures.